HECTOR

EVALUATION BOARD

USER GUIDE
1.3

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 644052

HECTOR HARDWARE ENABLED CRYPTO AND RANDOMNESS

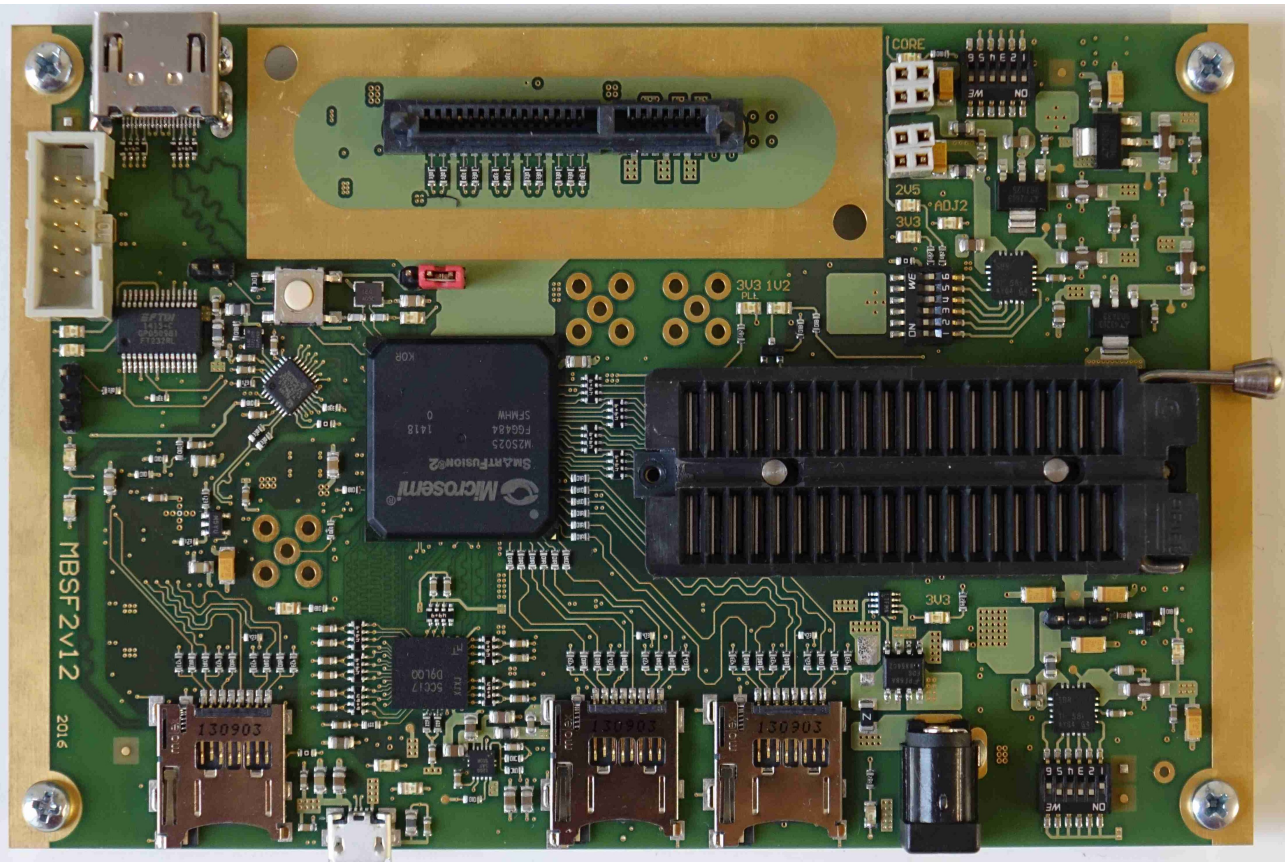
Content

Overview

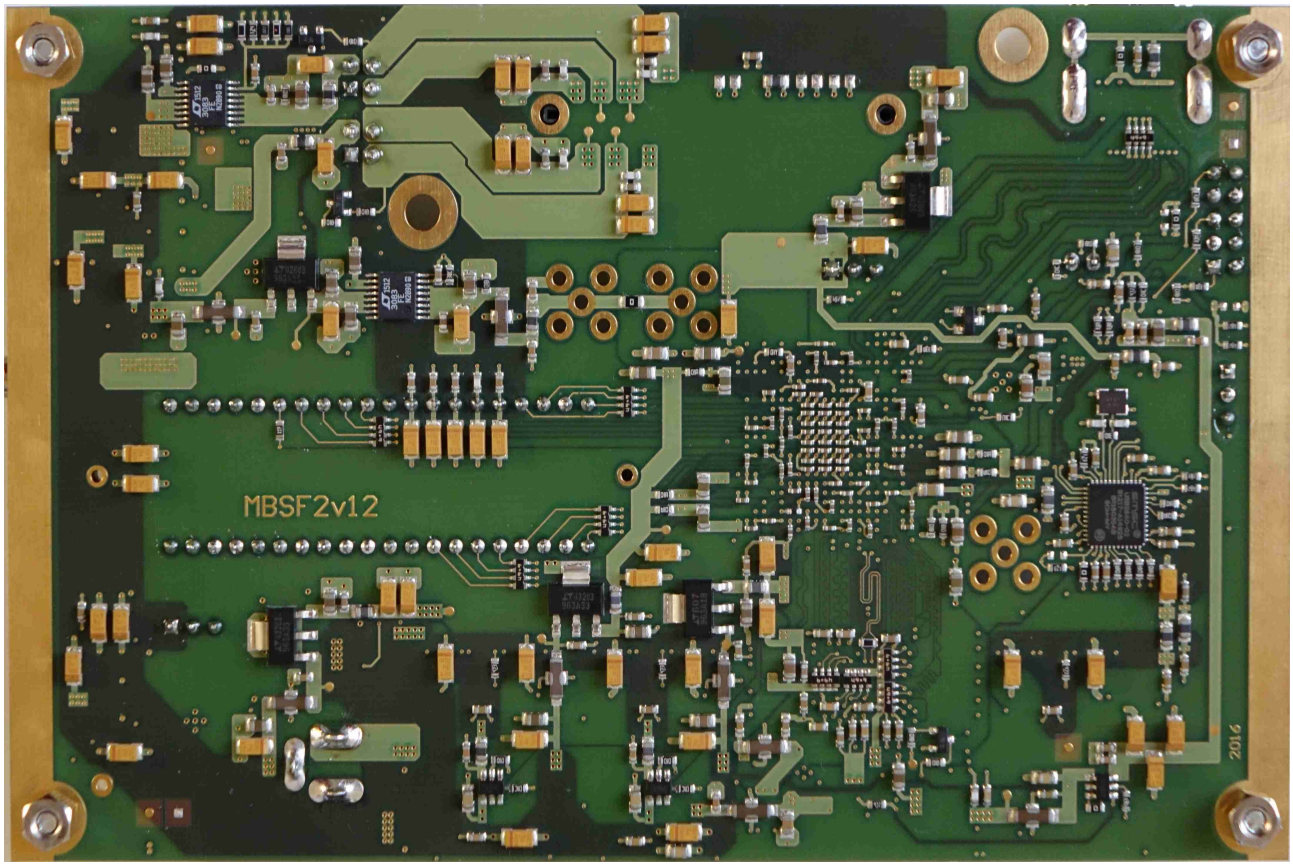
System description

The HECTOR Evaluation Board version 1.1/1.2 has similar architecture to the HECTOR Demonstrator and includes these hardware components:

- SoC FPGA, an FPGA with embedded ARM processor
- 512Mb RAM
- three different connectors for a daughter board
- three slots for external microSD FLASH card
- USB and UART communication interfaces
- a dedicated power supply port
- an SMA connector for triggering
- two SMA connectors for FPGA power consumption measurement

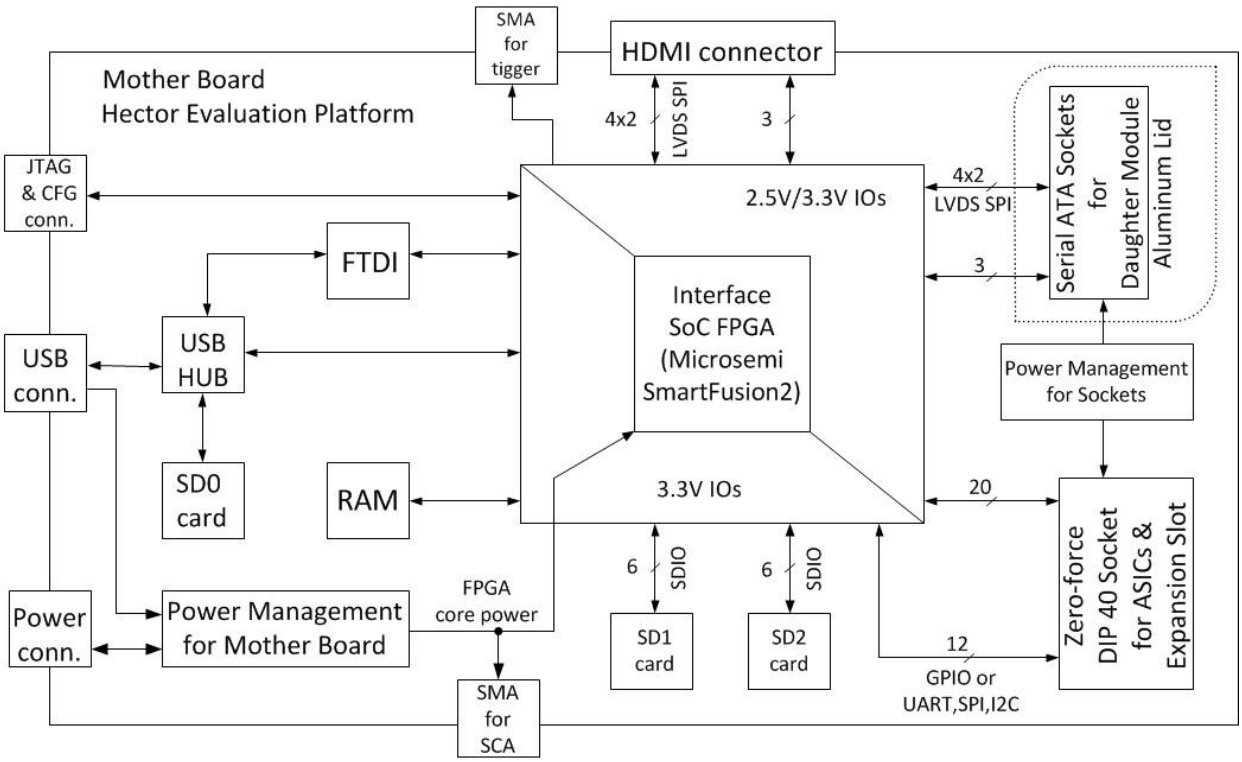


HECTOR Evaluation Board version 1.2 top side



HECTOR Evaluation Board version 1.2 bottom side

Architecture



HECTOR Evaluation Board version 1.1/1.2 architecture

The Microsemi SmartFusion2 SoC FPGA is used as reconfigurable platform in the HECTOR Evaluation Board version 1.1/1.2. It contains an embedded ARM processor with embedded FLASH and RAM memories, reasonable amount of FPGA logic elements, USB/UART interfaces.

As depicted in the previous figure, the HECTOR Evaluation Board consists of:

- SoC FPGA: Microsemi(r) SmartFusion(r)2 M2S025-FGG484
  - 27,696 logic blocks
  - 34 Math Blocks (18x18)
  - 6 PLLs
  - 64kB RAM
  - 256kB eNVM (FLASH for ARM)
  - USB, UART, I2C, SPI
  - 592kbits fabric memory
- Two SD-cards connected to the FPGA fabric
- USB hub
- FTDI virtual serial port interface
- SD-card connected to the USB hub

Evaluation Board kit

The HECTOR Evaluation Board kit includes:

- HECTOR Evaluation Board 1 - Mother Board version 1.1/1.2 equipped with Microsemi(r) SmartFusion(r)2 M2S025-FGG484
- (optional) HECTOR Evaluation Module 1 - Daughter Board equipped with Microsemi(r) SmartFusion(r)2 M2S025FGG484
- (optional) HECTOR Evaluation Module 2 - Daughter Board equipped with Xilinx(r) Spartan(r)6 XC6SLX16-2FTG256
- USB A – micro USB B cable
- 5V power supply
- Microsemi(r) FlashPro4 programmer, USB A – mini USB B cable

Contact

The HECTOR Evaluation Board is developed, manufactured and supplied by:

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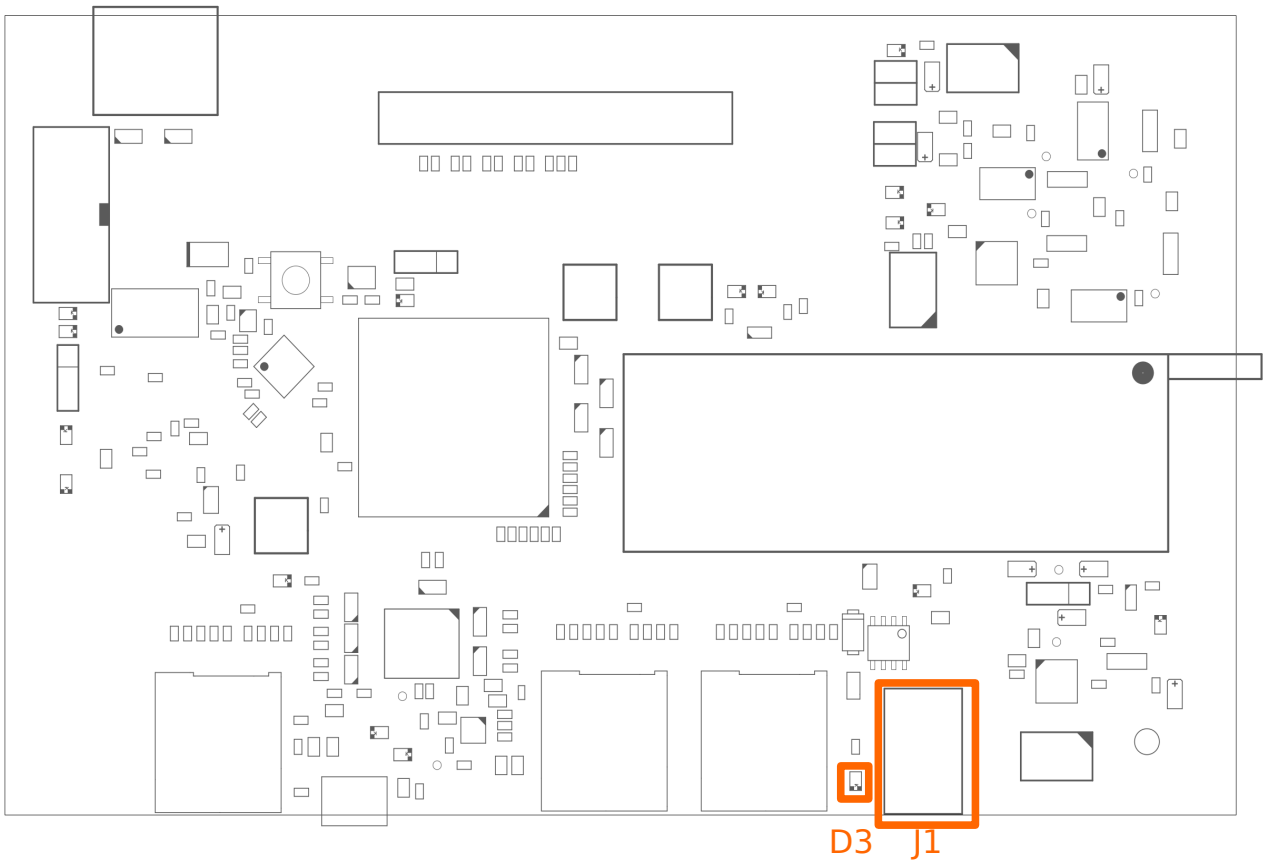
web: http://www.micronic.sk

Power

Mother board power

The mother board is powered from a dedicated 5V power supply.



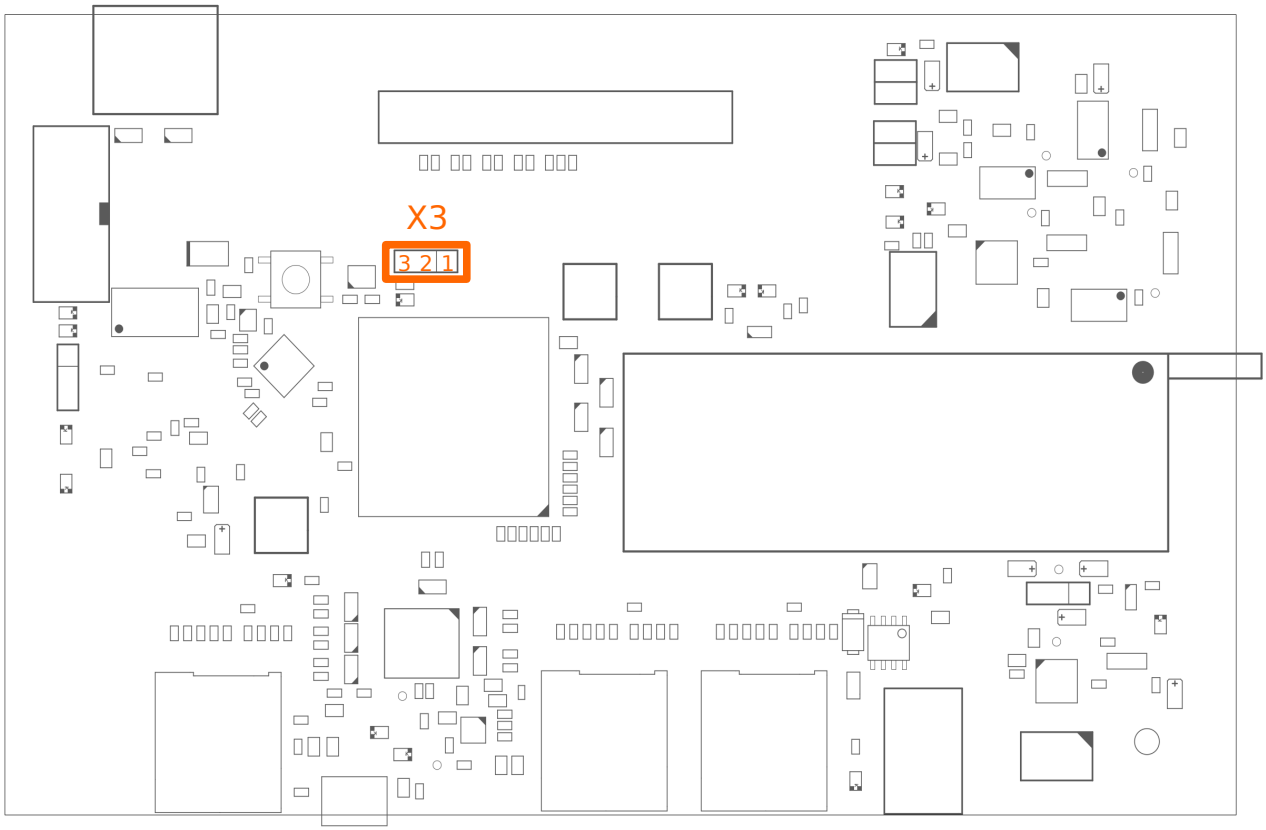
To power the mother board from a dedicated power supply:

1. Attach a 5V power supply to the connector J1.

2. The green LED D3 should light on.

FPGA power

The core is powered by 1.2V. The PLLs are powered from a dedicated 3.3V power line, decoupled from other 3.3V logic.

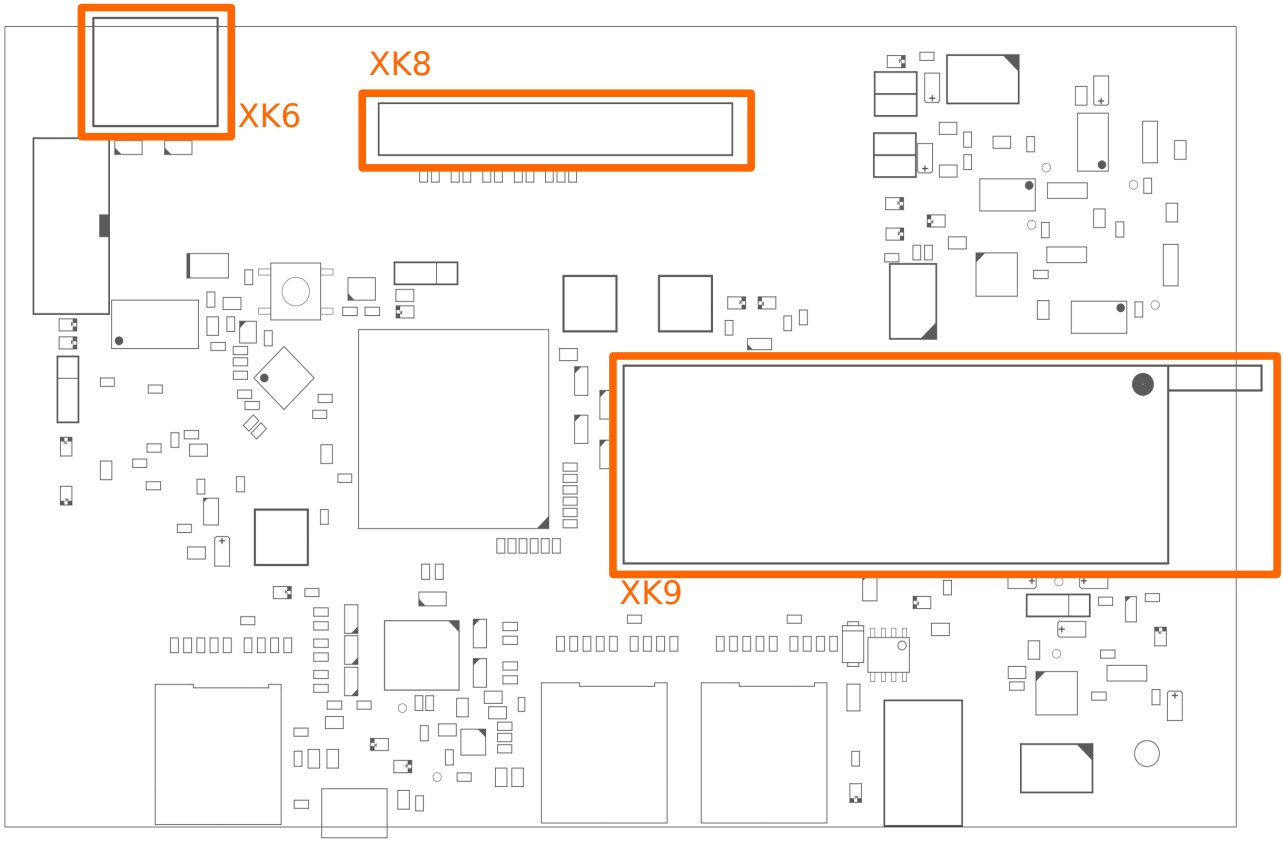


I/O Banks powering

I/O Bank 0	1.8V
I/O Bank 1	3.3V
I/O Bank 2	3.3V
I/O Bank 3	3.3V
I/O Bank 4	2.5V when X3 set to 1-2 3.3V when X3 set to 2-3
I/O Bank 5	not used, not powered
I/O Bank 6	2.5V
I/O Bank 7	3.3V

Connecting the daughter board

The mother board provides three optional connectors to attach the daughter board.



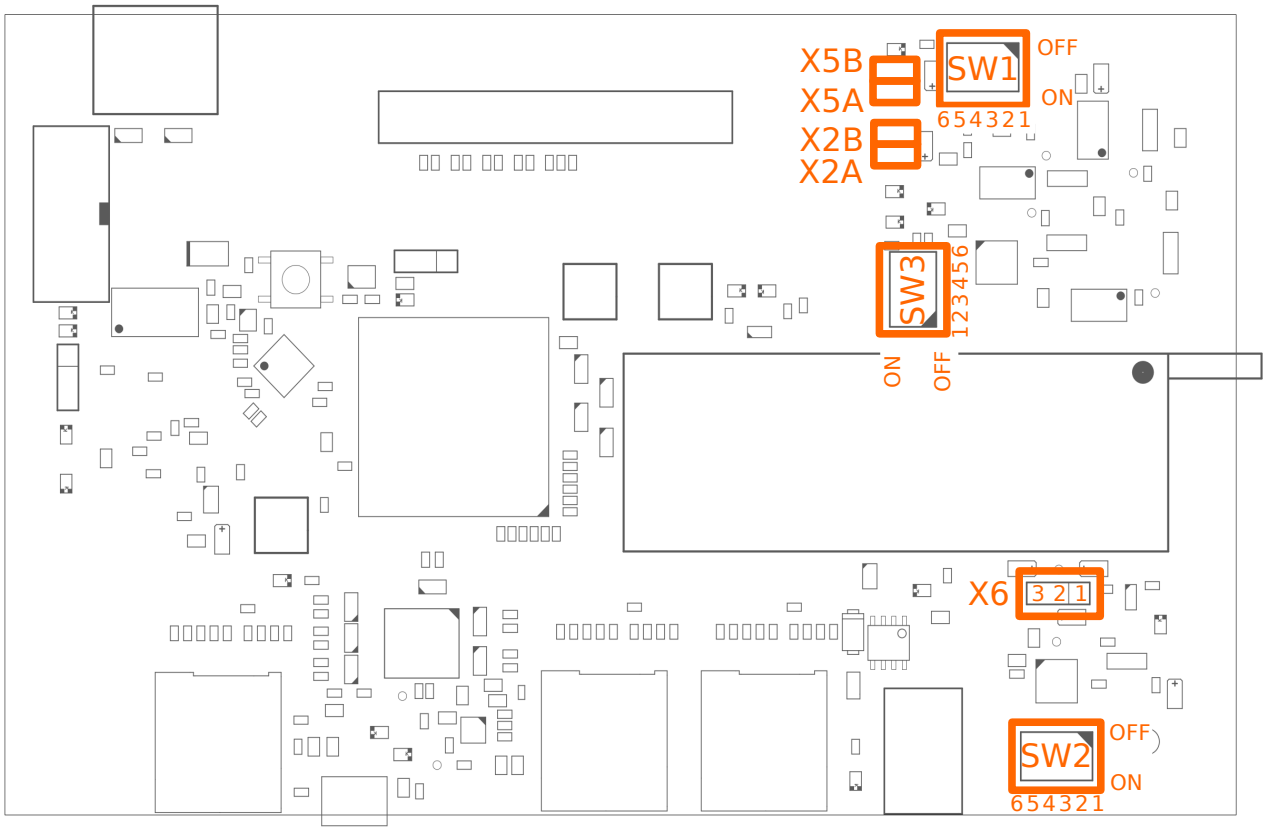
Daughter board connectors

		data		power ports
		differential pairs	single ended signals	
XK6	HDMI form	4	3	1
XK8	SATA form	4	3	5
XK9	40 pin zero force connector	0	32	5

XK8 (SATA form) and XK6 (HDMI form) connectors are not pin compatible with the respective standards. **Avoid the possibility to connect a SATA or HDMI compliant device to the HECTOR Evaluation Board!**

Daughter board power

There are many options to power-supply the daughter board. There are two fixed voltages and three adjustable regulators to power-supply the daughter board.



Powering the daughter board

X2A	ADJ2_REG / DUT_ADJ2	0.9-3.3V
X2B	REG_3V3 / DUT_3V3	3.3V
X5A	REG_2V5 / DUT_2V5	2.5V
X5B	REG_CORE / DUT_CORE	0.9-1.5V
X6 1-2	5V_INPUT / DUT_ADJ1	5V
X6 2-3	ADJ1_REG / DUT_ADJ1	0.9-3.3V

The SW1 switch adjusts the REG_CORE voltage.

Vout	1	2	3	4	5	6
0,90	on	on	on	on	on	DNC
1,00	on	on	on	on	off	
1,10	on	on	on	off	off	

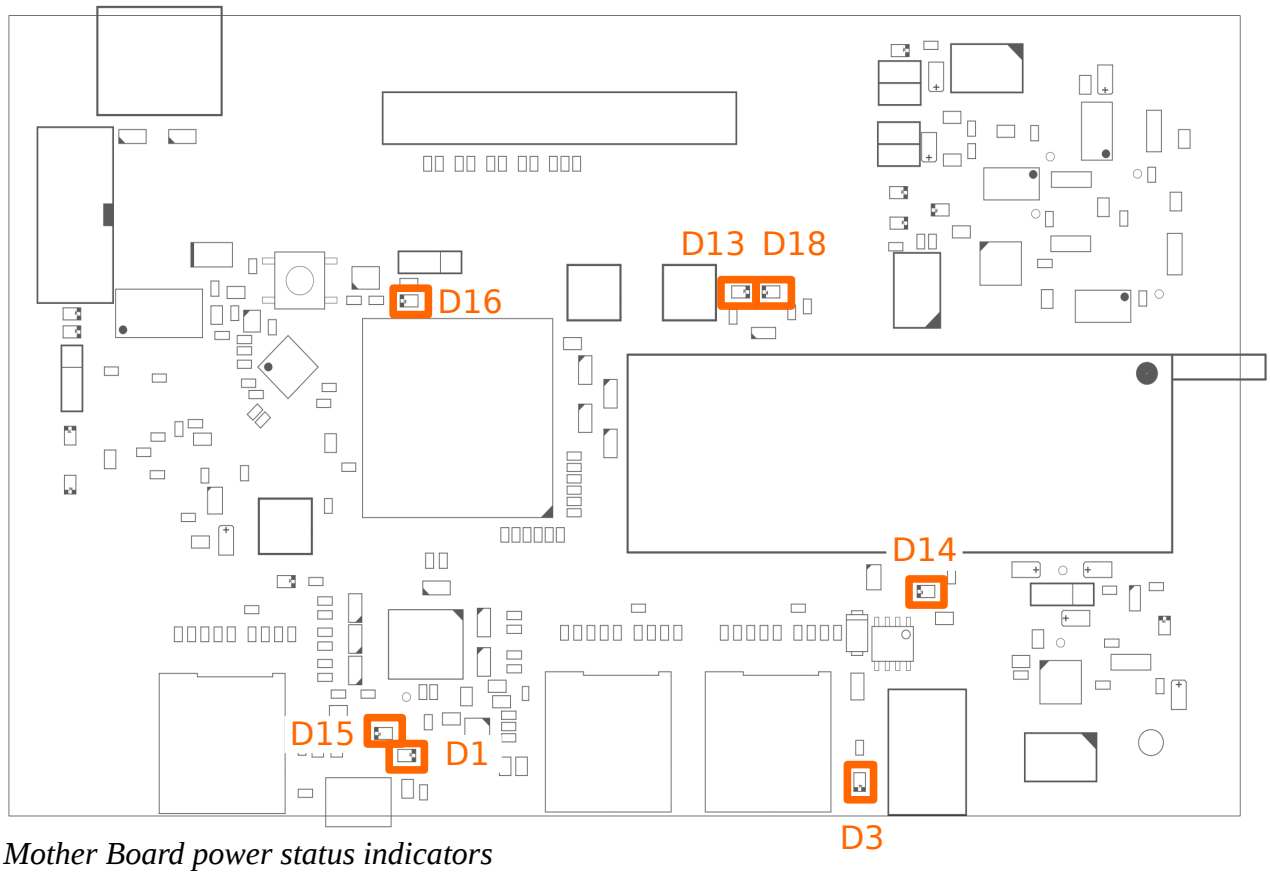
Vout	1	2	3	4	5	6
1,20	on	on	off	off	off	DNC
1,50	on	off	off	off	off	

The SW2 and SW3 switches adjust the ADJ1_REG and ADJ2_REG voltages respectively.

Vout	1	2	3	4	5	6
0.90	off	off	on	off	off	off
0.95	off	off	on	off	off	on
1.00	off	off	on	off	on	off
1.05	off	off	on	off	on	on
1.10	off	off	on	on	off	off
1.15	off	off	on	on	off	on
1.20	off	off	on	on	on	off
1.25	off	off	on	on	on	on
1.30	off	on	off	off	off	off
1.35	off	on	off	off	off	on
1.40	off	on	off	off	on	off
1.45	off	on	off	off	on	on
1.50	off	on	off	on	off	off
1.55	off	on	off	on	off	on
1.60	off	on	off	on	on	off
1.65	off	on	off	on	on	on
1.70	off	on	on	off	off	off
1.75	off	on	on	off	off	on
1.80	off	on	on	off	on	off
1.85	off	on	on	off	on	on
1.90	off	on	on	on	off	off
1.95	off	on	on	on	off	on
2.00	off	on	on	on	on	off
2.05	off	on	on	on	on	on
2.10	on	off	off	off	off	off
2.15	on	off	off	off	off	on

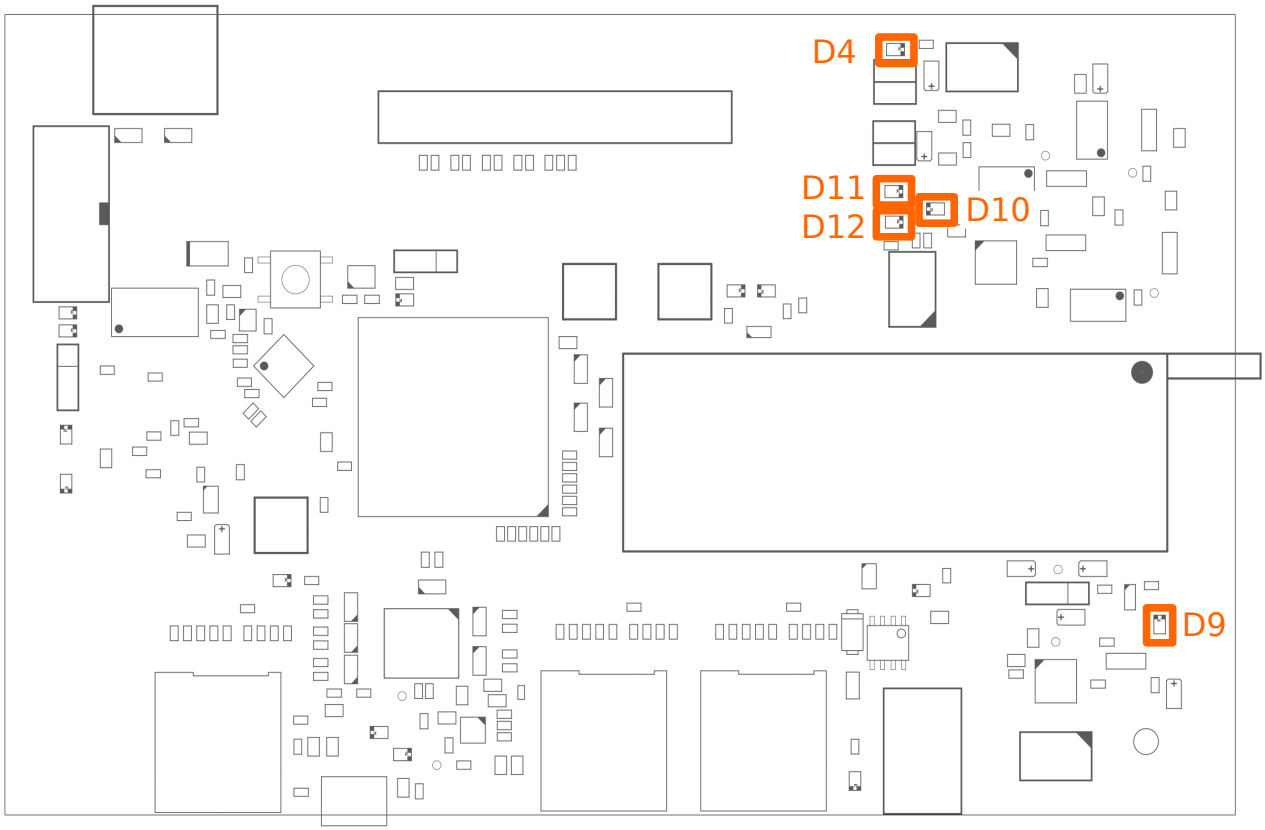
Vout	1	2	3	4	5	6
2.20	on	off	off	off	on	off
2.25	on	off	off	off	on	on
2.30	on	off	off	on	off	off
2.35	on	off	off	on	off	on
2.40	on	off	off	on	on	off
2.45	on	off	off	on	on	on
2.50	on	off	on	off	off	off
2.55	on	off	on	off	off	on
2.60	on	off	on	off	on	off
2.65	on	off	on	off	on	on
2.70	on	off	on	on	off	off
2.75	on	off	on	on	off	on
2.80	on	off	on	on	on	off
2.85	on	off	on	on	on	on
2.90	on	on	off	off	off	off
2.95	on	on	off	off	off	on
3.00	on	on	off	off	on	off
3.05	on	on	off	off	on	on
3.10	on	on	off	on	off	off
3.15	on	on	off	on	off	on
3.20	on	on	off	on	on	off
3.25	on	on	off	on	on	on
3.30	on	on	on	off	off	off
3.35	on	on	on	off	off	on
3.40	on	on	on	off	on	off
3.45	on	on	on	off	on	on
3.50	on	on	on	on	off	off

Power status indicators



Mother Board power status indicators

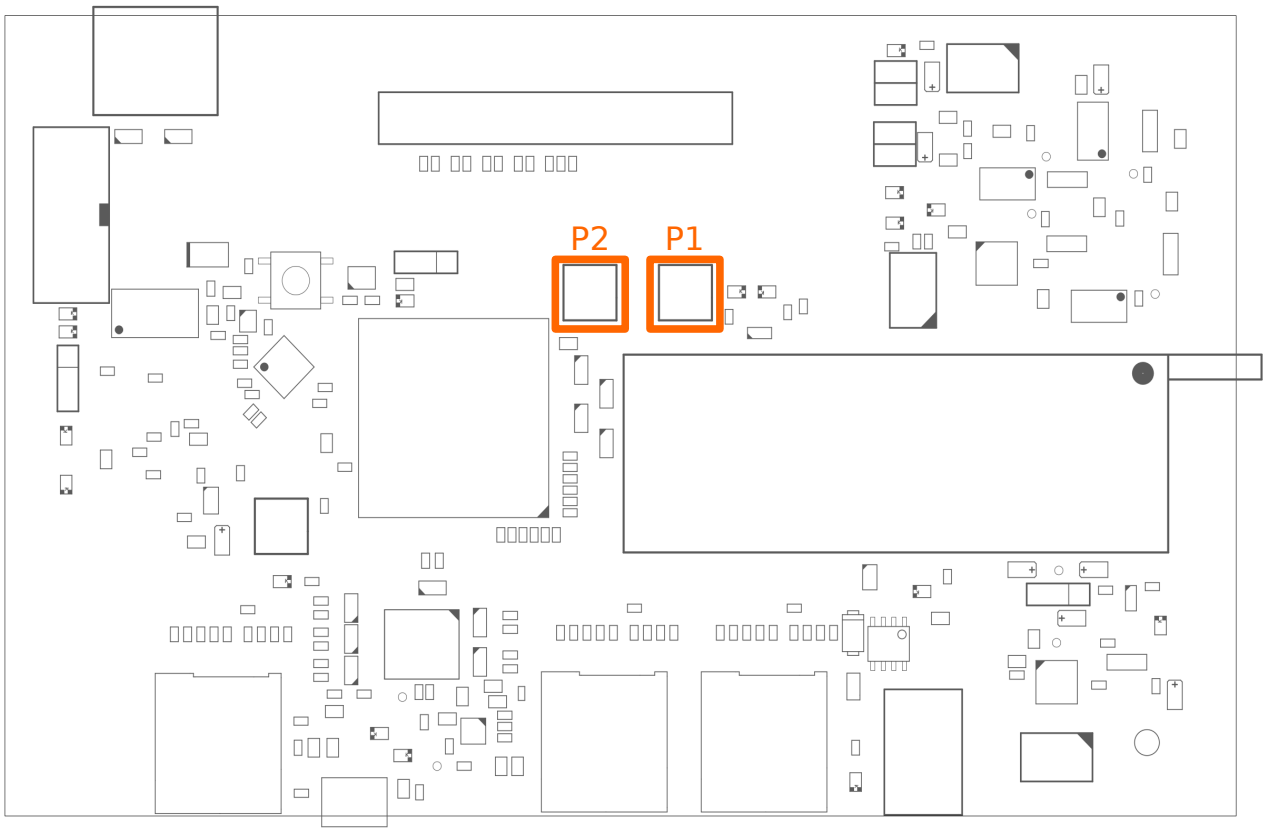
D1	red	USB voltage error
D3	green	Mother Board voltage 5V OK
D13	green	Mother Board voltage 3.3V for SoC PLLs OK
D14	green	Mother Board voltage 3.3V OK
D15	green	Mother Board voltage 1.8V OK
D16	green	Mother Board voltage 2.5V OK
D18	green	Mother Board voltage 1.2V OK



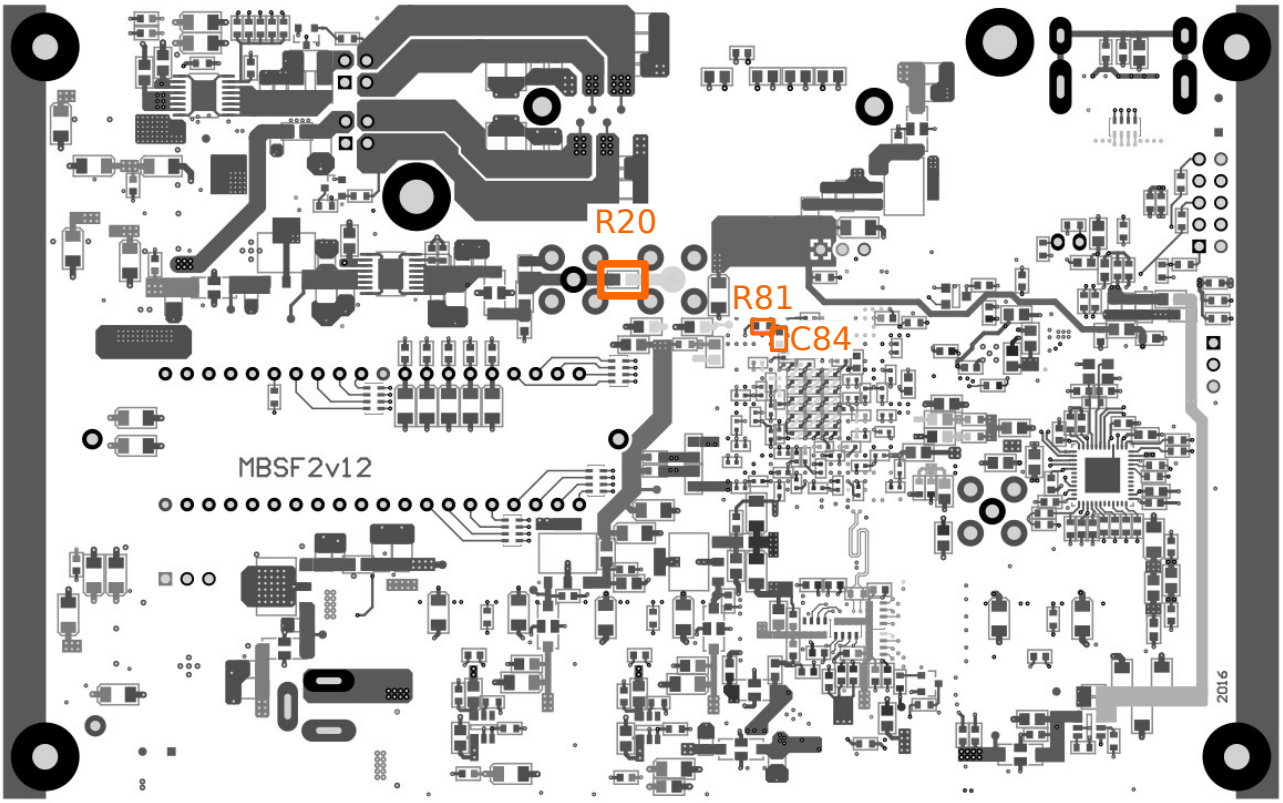
Daughter Board power status indicators

D4	green	Daughter Board core voltage OK
D9	green	Daughter Board adjustable voltage ADJ1 OK
D10	green	Daughter Board adjustable voltage ADJ2 OK
D11	green	Daughter Board voltage 2.5V OK
D12	green	Daughter Board voltage 3.3V OK

Power consumption



Connectors for the SoC FPGA core power consumption measurement

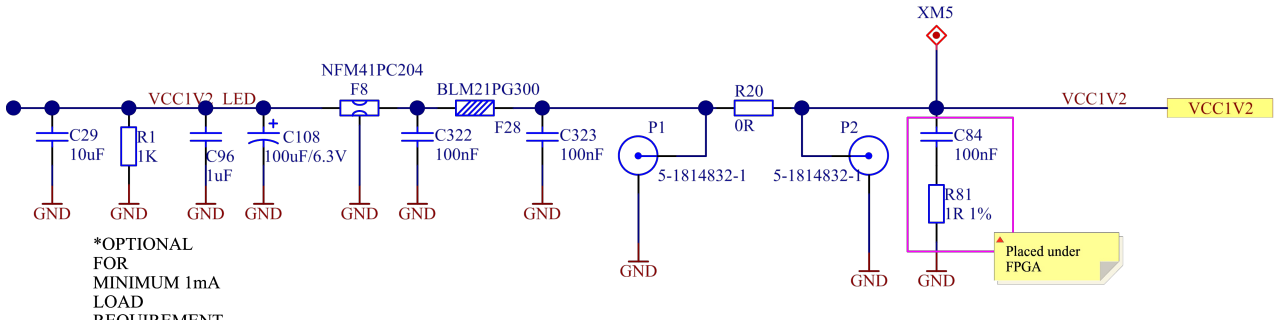


Passive components in the SoC FPGA core power line

To measure the mother board SoC FPGA power consumption:

1. either replace the R20 zero ohm resistor with a resistor of a suitable value

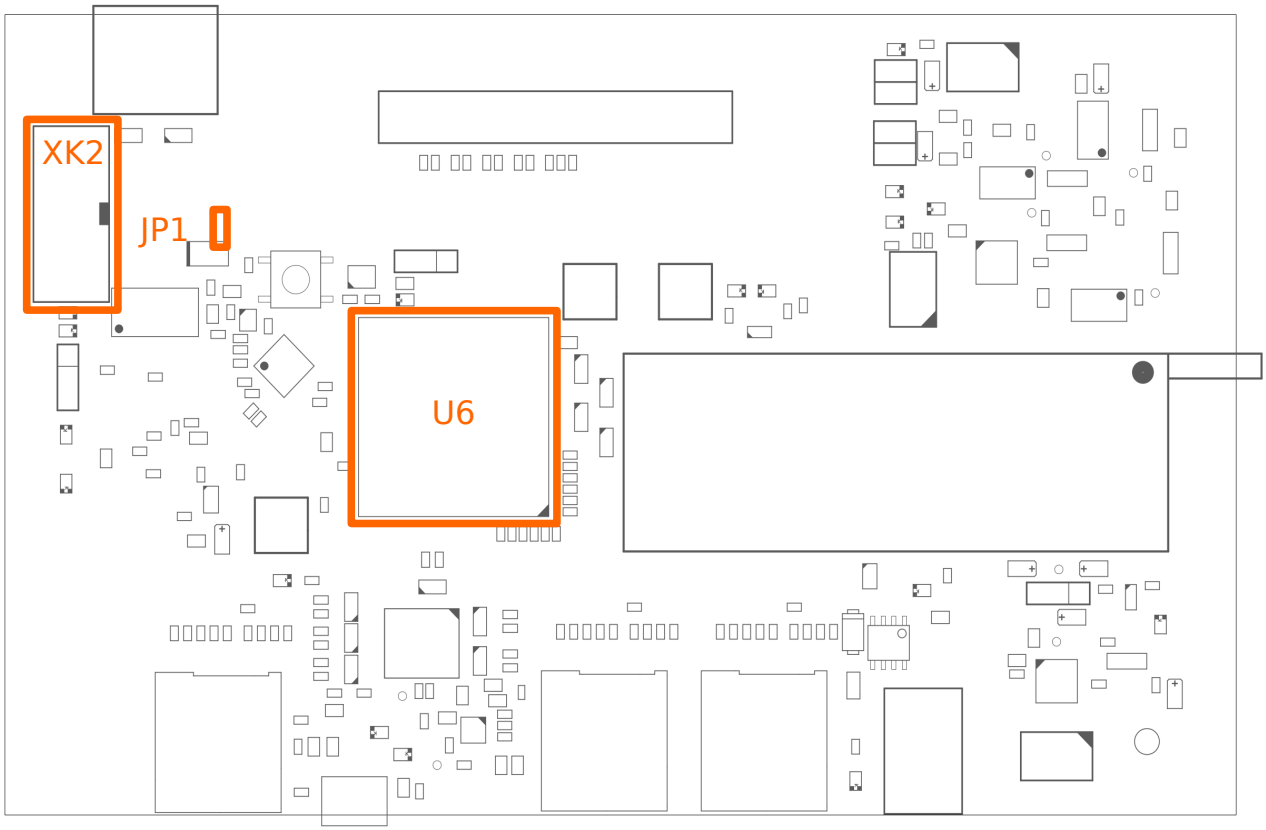
2. or remove the R20 zero ohm resistor and attach a current probe between P1 and P2.



Developing

FPGA programming

The SoC FPGA U6 Microsemi(r) SmartFusion(r)2 M2S090-FG484 is the heart of the Mother Board. It consists of an FPGA and an ARM. The FPGA is in field reprogrammable.



To program the FPGA U6:

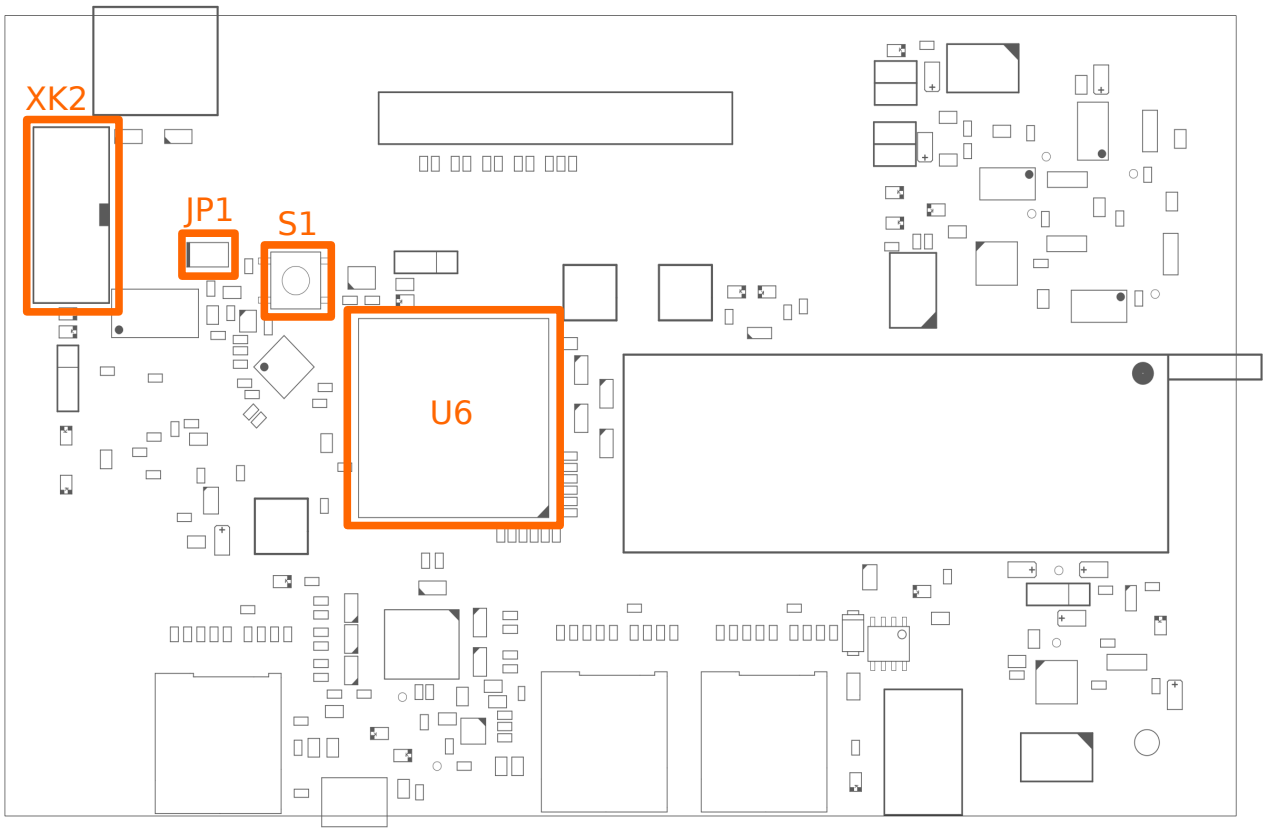
1. Check if the jumper JP1 is in the open position.

2. Attach the Microsemi(r) FlashPro4 programmer to the connector XK2.

3. Program the FPGA with an appropriate project using the Libero System-on-Chip software tools.

ARM debugging

The other part of the SoC FPGA is the ARM.



To debug the ARM U6:

1. Check if the jumper JP1 is in the open position.[1]

2. Attach the Microsemi(r) FlashPro4 programmer to the connector XK2.

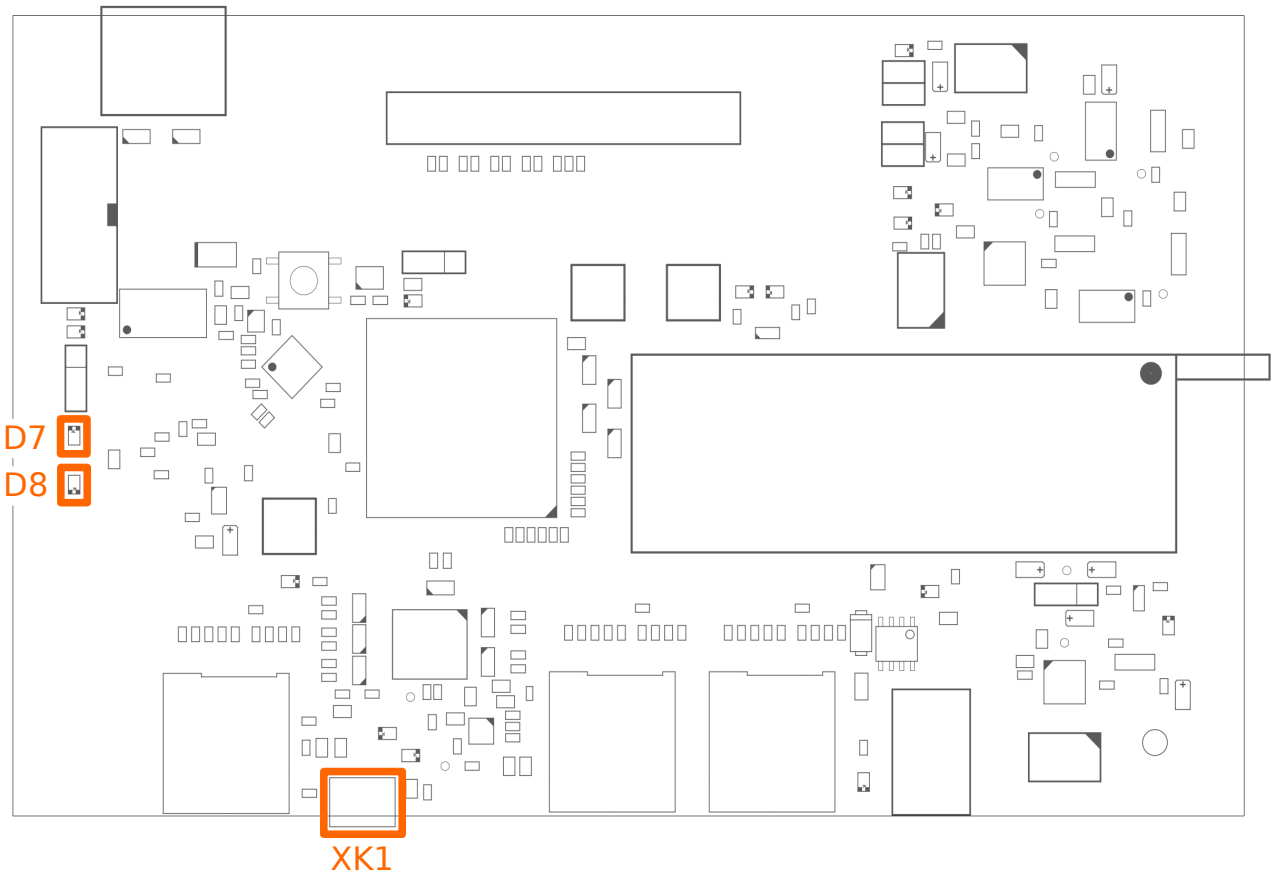
3. Launch the Microsemi(r) SoftConsole 4.0, open an appropriate project and start debugging.

To reset the ARM U6 push the button S1.

1 For the recommended setup for microcontroller debugging using tools such as IAR® or KEIL™ look into the *SmartFusion2 and IGLOO2 Programming User Guide* (http://www.microsemi.com/document-portal/doc_view/132014-ug0451-igloo2-and-smartfusion2-programming-user-guide) Chapter 2.

Communicating

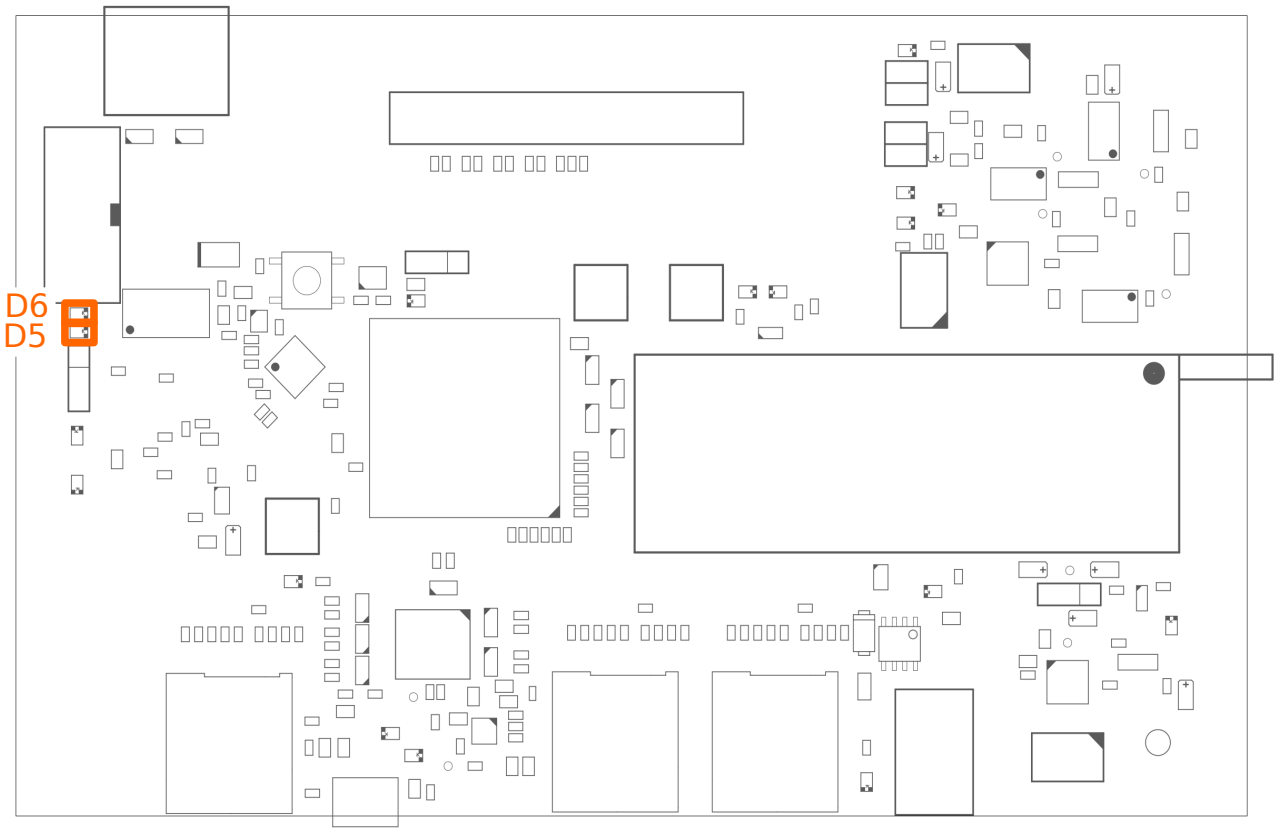
USB



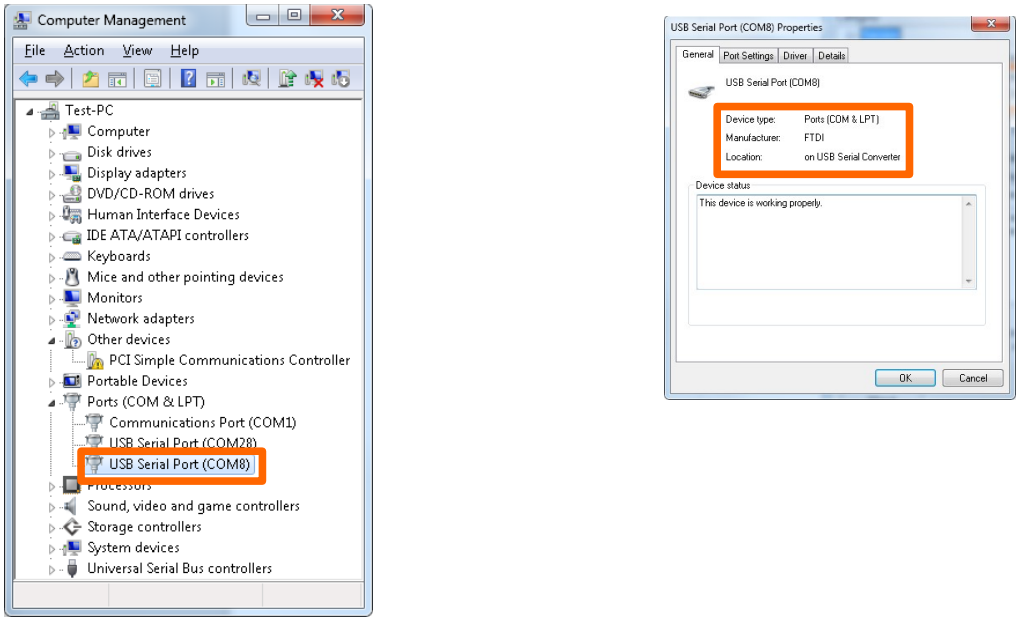
Attach the HECTOR Evaluation board to your computer using the micro USB B connector XK1.

UART

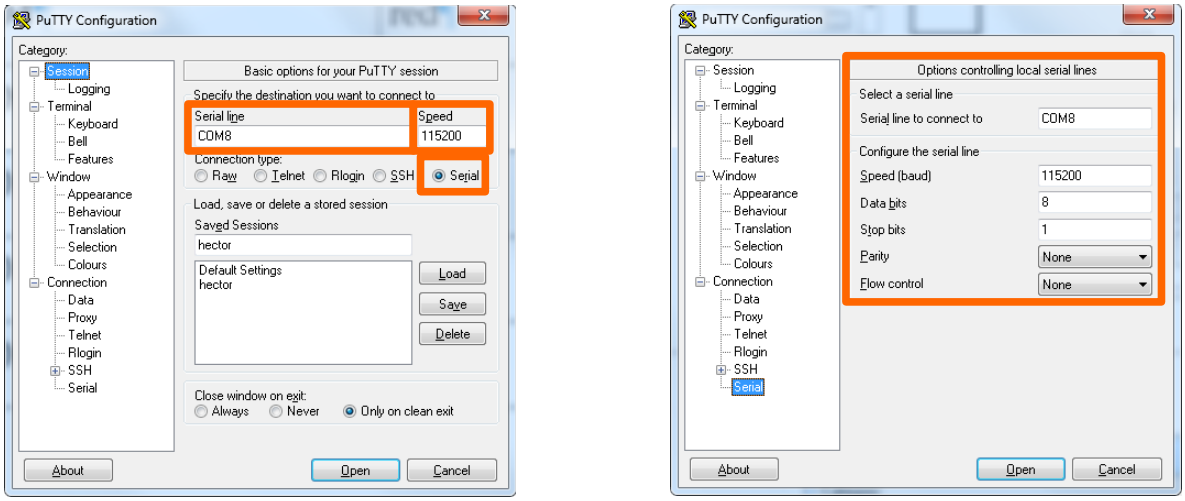
The ARM UART1 hardware serial port is connected via FTDI's FT232 USB to serial converter to the USB hub. For proper function the virtual COM port driver (available at http://www.ftdichip.com/Drivers/VCP.htm) must be installed on the computer.



The green D5 LED indicates incomming communication (RX) and the red D6 indicates outgoing communication (TX)

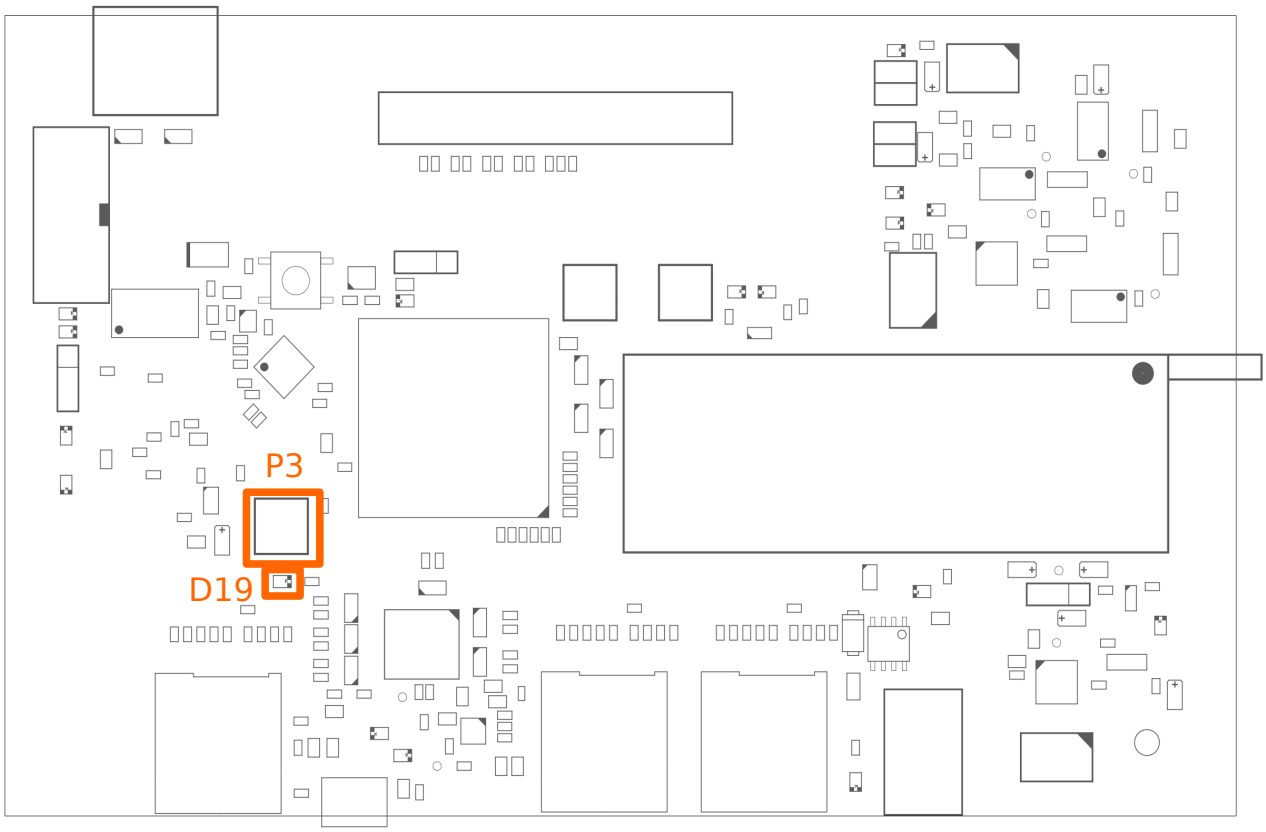


A new serial port appears in the Device Manager after attaching the HECTOR Evaluation Board to the computer. The number of the port may vary.



Configuration of the terminal using PuTTY (available at http://www.chiark.greenend.org.uk/~sgtatham/putty/download.html).

FPGA I/Os



The green LED D19 is connected to the FPGA pin E21.

The inner pin of the SMA connector P3 is connected to the FPGA pin G21. The connector is intended for triggering.

Appendix A

Test daughter board for the ZIF connector pinout (preliminary)

DB_ZIF_TEST signal name	ZIF40 connector pin number	schematics signal name	SoC FPGA pin number
S14	01	D3_IO10 SCKT_IO10 D3_GPIO10	R3
S13	02	D3_IO20 SCKT_IO20 D3_GPIO20	R1
S12	03	D3_IO15 SCKT_IO15 D3_GPIO15	R2
S11	04	D3_IO03 SCKT_IO03 D3_GPIO03	T4
S10	05	D3_IO09 SCKT_IO09 D3_GPIO09	T3
S09	06	D3_IO14 SCKT_IO14 D3_GPIO14	L3
S08	07	D3_IO13 SCKT_IO13 D3_GPIO13	M3
S07	08	D3_IO04 SCKT_IO04 D3_GPIO04	L4
S06	09	D3_IO05 SCKT_IO05 D3_GPIO05	L5
S05	10	D3_IO02 SCKT_IO02 D3_GPIO02	P4
GND	11	GND	
	12	DUT_PWR_ADJ2	
3V3	13	DUT_3V3	
	14	DUT_2V5	
	15	DUT_CORE	

DB_ZIF_TEST signal name	ZIF40 connector pin number	schematics signal name	SoC FPGA pin number
	16	DUT_CORE	
S04	17	D3_IO29 SPI_MOSI SPI_1_SDO	L21
S03	18	D3_IO30 SPI_MISO SPI_1_SDI	M22
S02	19	D3_IO27 SPI_CLK SPI_1_CLK	M21
S01	20	D3_IO28 SPI_CS SPI_1_SS0	L20
D01	21	D3_IO26 I2C_CLK I2C_SCL	G16
D02	22	D3_IO25/SCKT_IO25/ I2C_DATA I2C_SDA	G17
D03	23	D3_IO32 UART_TX UART_0_TXD	D21
D04	24	D3_IO31 UART_RX UART_0_RXD	C22
D05	25	D3_IO21 SCKT_IO21 D3_GPIO21	G2
D06	26	D3_IO23 SCKT_IO23 D3_GPIO23	F5
D07	27	D3_IO24 SCKT_IO24 D3_GPIO24	F6
D08	28	D3_IO22 SCKT_IO22 D3_GPIO22	E5
D09	29	D3_IO08 SCKT_IO08 D3_GPIO08	K4

DB_ZIF_TEST signal name	ZIF40 connector pin number	schematics signal name	SoC FPGA pin number
D10	30	D3_IO19 SCKT_IO19 D3_GPIO19	K2
D11	31	D3_IO01 SCKT_IO01 D3_GPIO01	K1
D12	32	D3_IO18 SCKT_IO18 D3_GPIO18	L2
D13	33	D3_IO17 SCKT_IO17 D3_GPIO17	M2
D14	34	D3_IO06 SCKT_IO06 D3_GPIO06	M1
D15	35	D3_IO12 SCKT_IO12 D3_GPIO12	N3
D16	36	D3_IO07 SCKT_IO07 D3_GPIO07	N1
D17	37	D3_IO16 SCKT_IO16 D3_GPIO16	P2
D18	38	D3_IO11 SCKT_IO11 D3_GPIO11	P1
	39	DUT_PWR_ADJ1	
GND	40	GND	